

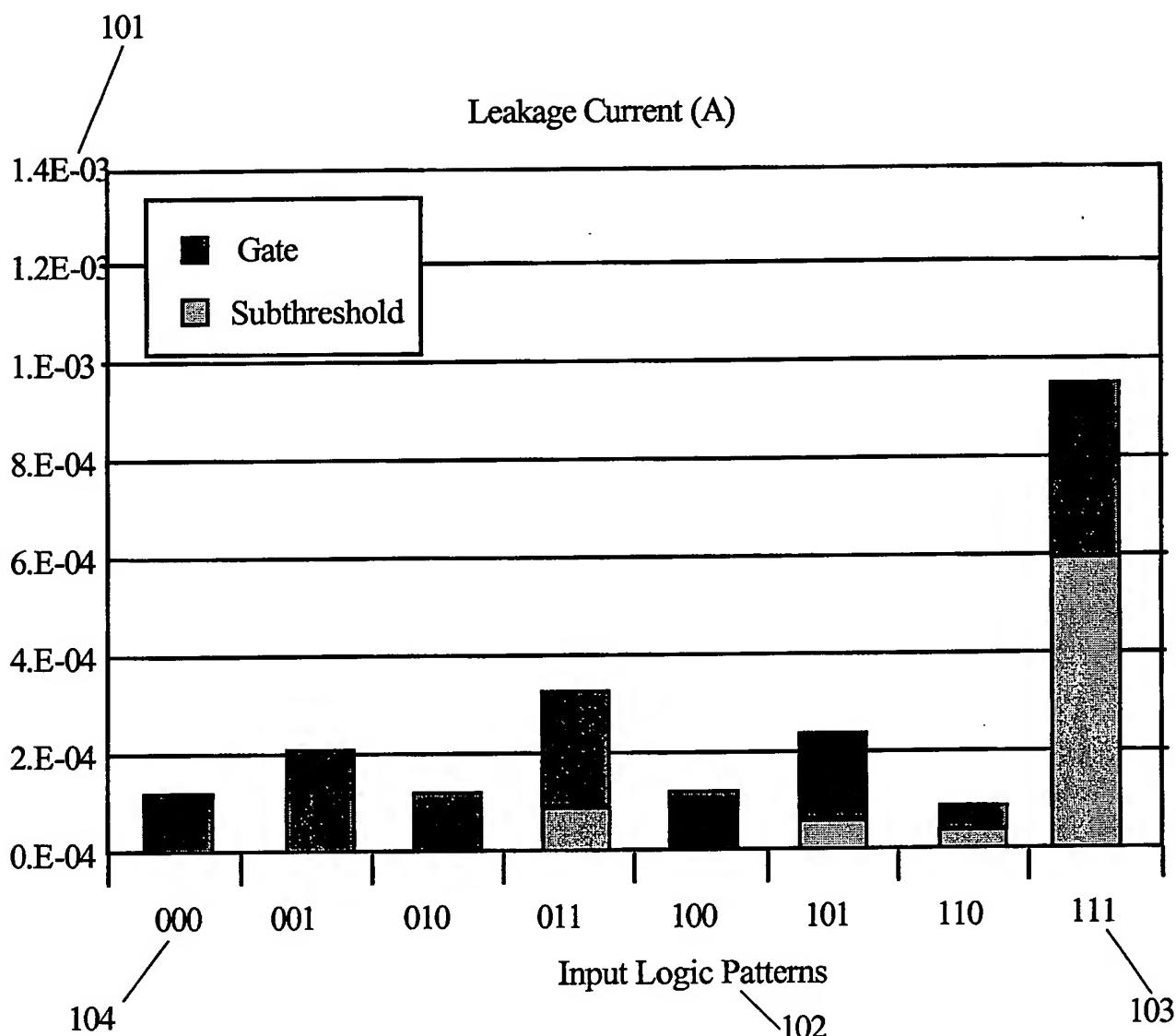
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FIG. 1

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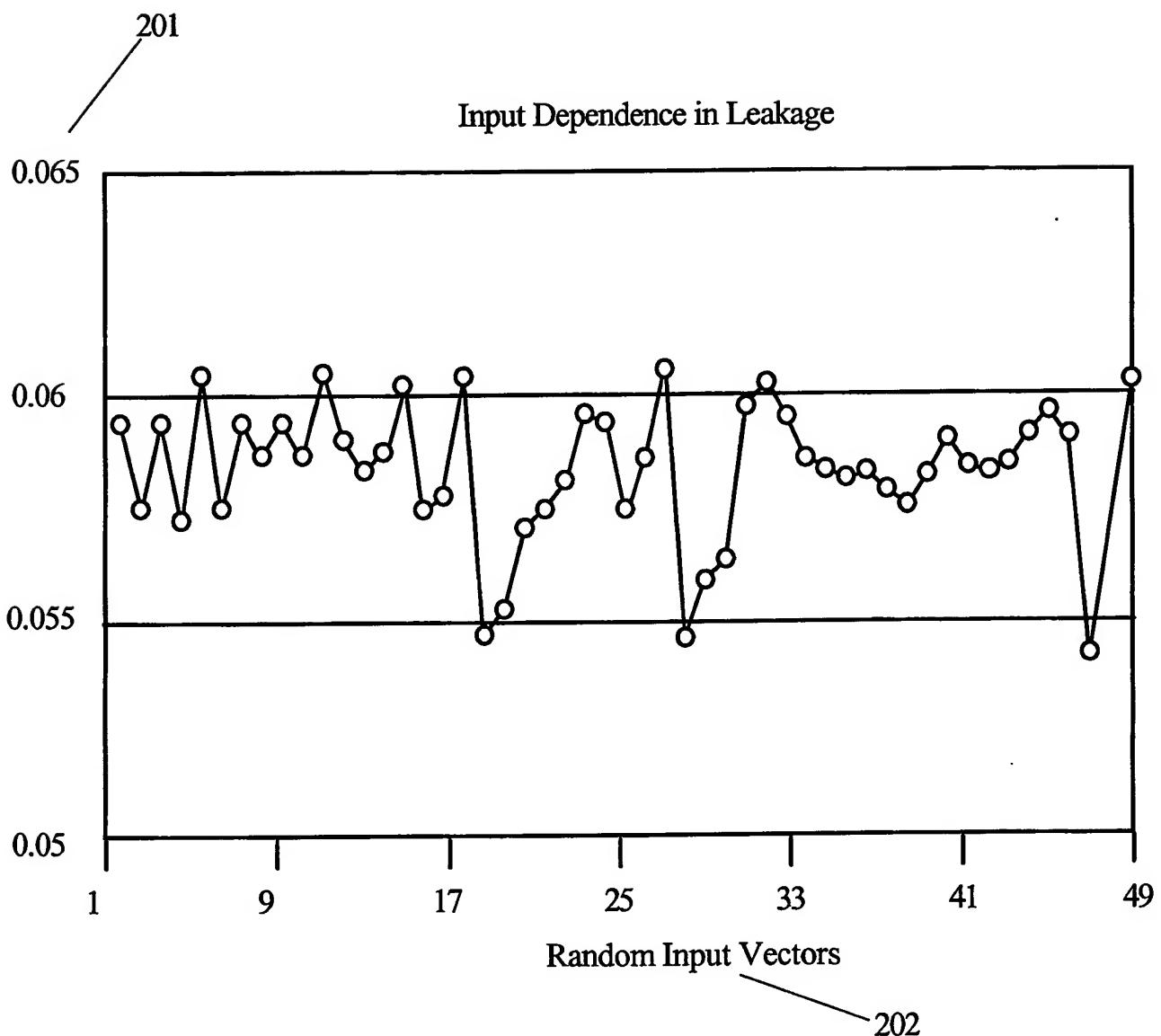


FIG. 2

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301	302	303	304	305	306
Circuit	# Cells	# inputs	$I_{max}$ (mA)	$I_{min}$ (mA)	cv.
c432	187	36	0.073899	0.0597	0.0237
c499	222	41	0.21463	0.153863	0.0337
c880	383	60	0.132035	0.095789	0.0335
c1355	566	41	0.173451	0.127854	0.0301
c1908	996	33	0.312824	0.210898	0.0610
c2670	11255	233	0.427436	0.325011	0.0363
c5311	2485	178	0.824406	0.670118	0.0279
c7752	3692	270	0.713998	0.665011	0.0483

FIG. 3

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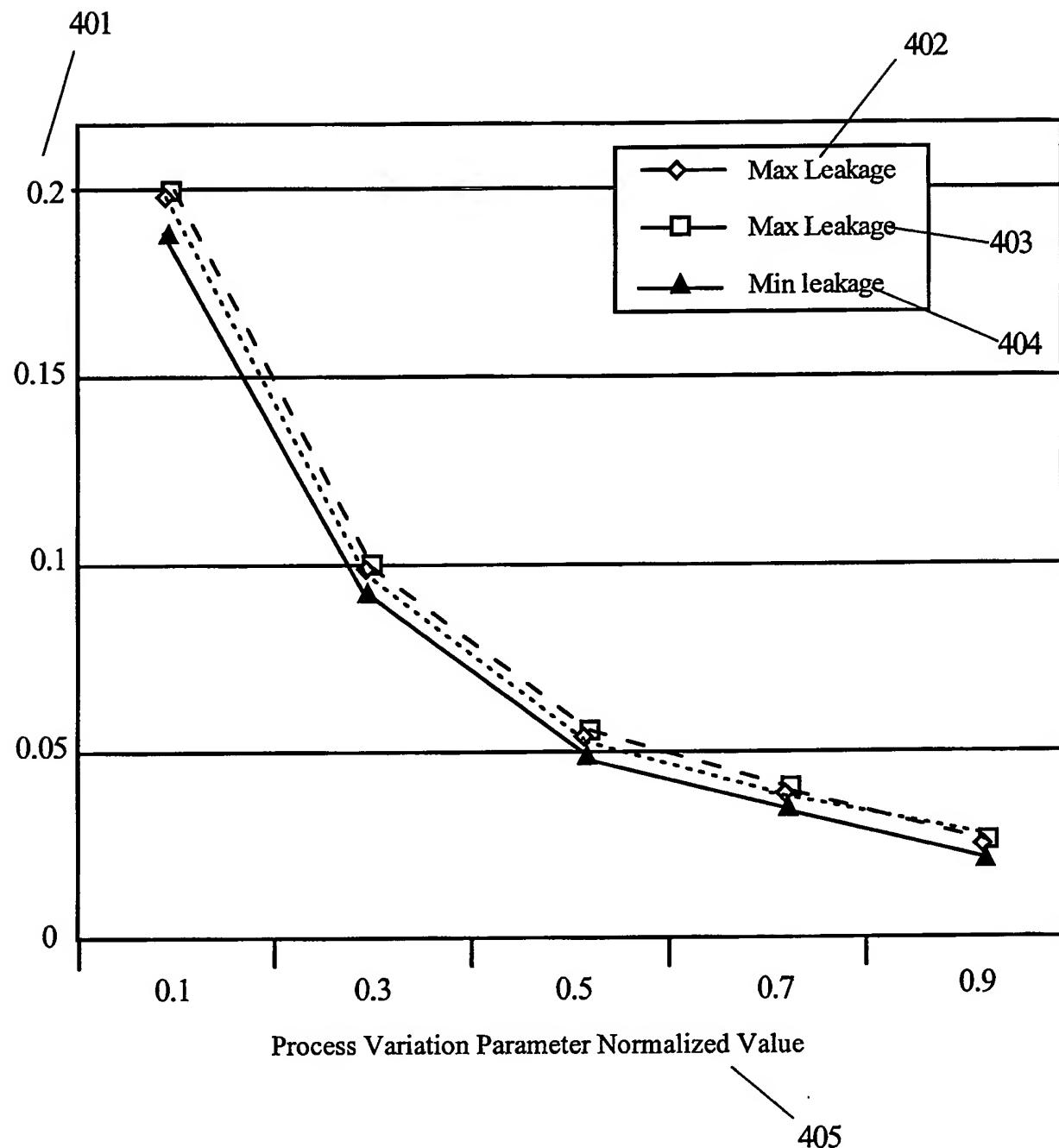


FIG. 4

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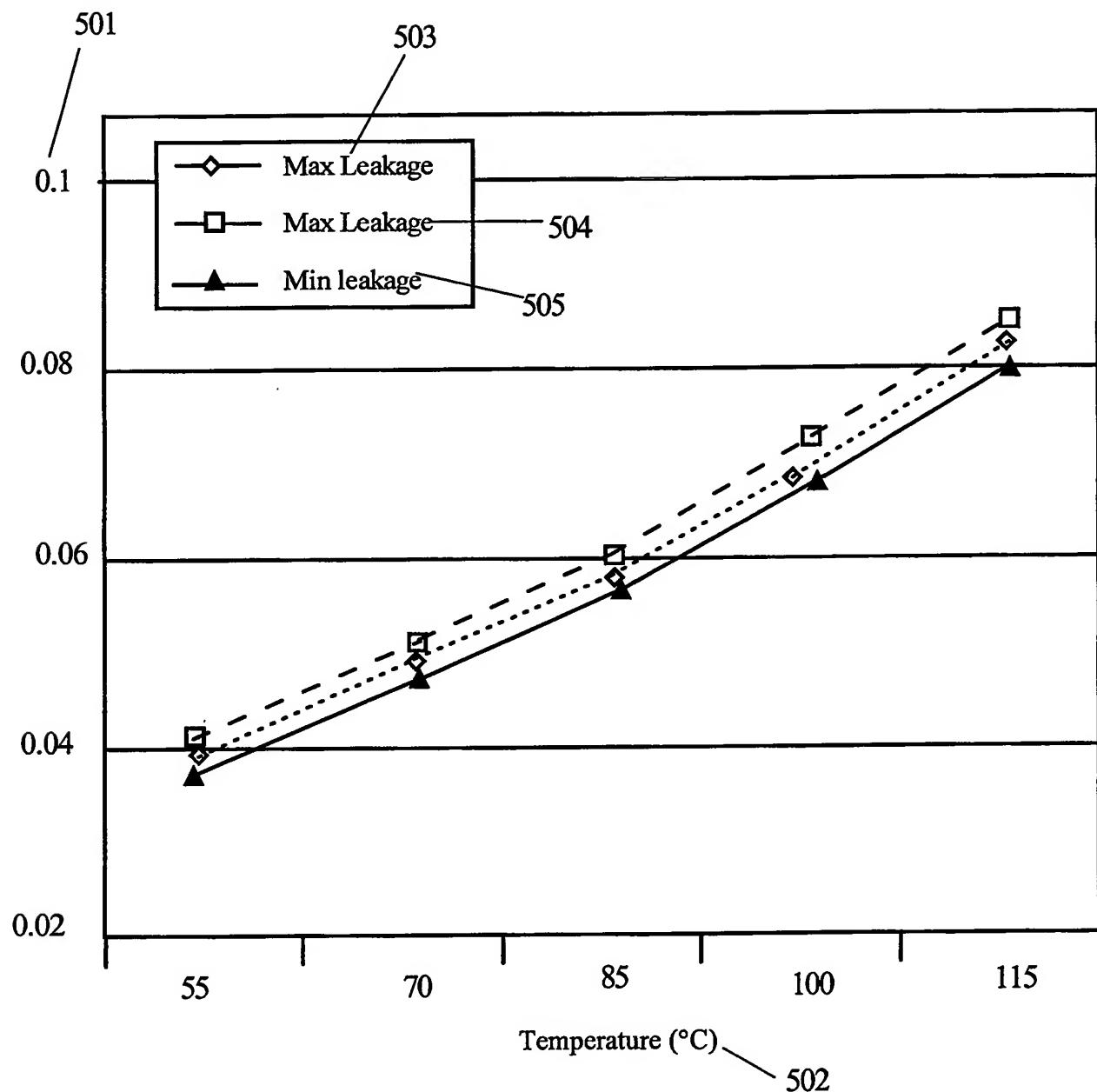


FIG. 5

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State	Gate leakage	Subthreshold Leakage	Total Leakage	State Occurrence Probability
00	$G_{00}$	$S_{00}$	$L_{00}=G_{00}+S_{00}$	$(1-P_1)(1-P_2)$
01	$G_{01}$	$S_{01}$	$L_{01}=G_{01}+S_{01}$	$(1-P_1)P_2$
10	$G_{10}$	$S_{10}$	$L_{10}=G_{10}+S_{10}$	$P_1(1-P_2)$
11	$G_{11}$	$S_{11}$	$L_{11}=G_{11}+S_{11}$	$P_1P_2$

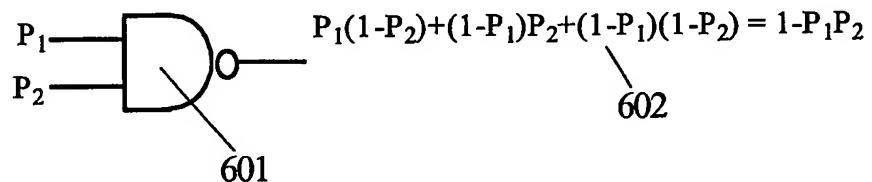


FIG. 6

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Circuit	Ave Leakage(W)	SP Method (W)	Rel. Error(%)
c432	0.06599	0.06800	3.056
c499	0.17885	0.17786	-0.556
c880	0.10857	0.10927	0.643
c1355	0.13828	0.14236	2.950
c1908	0.22508	0.21437	-4.758
c2670	0.34197	0.34638	1.290
c5311	0.70782	0.71171	0.549
c7752	0.99772	0.97618	-2.158

FIG. 7

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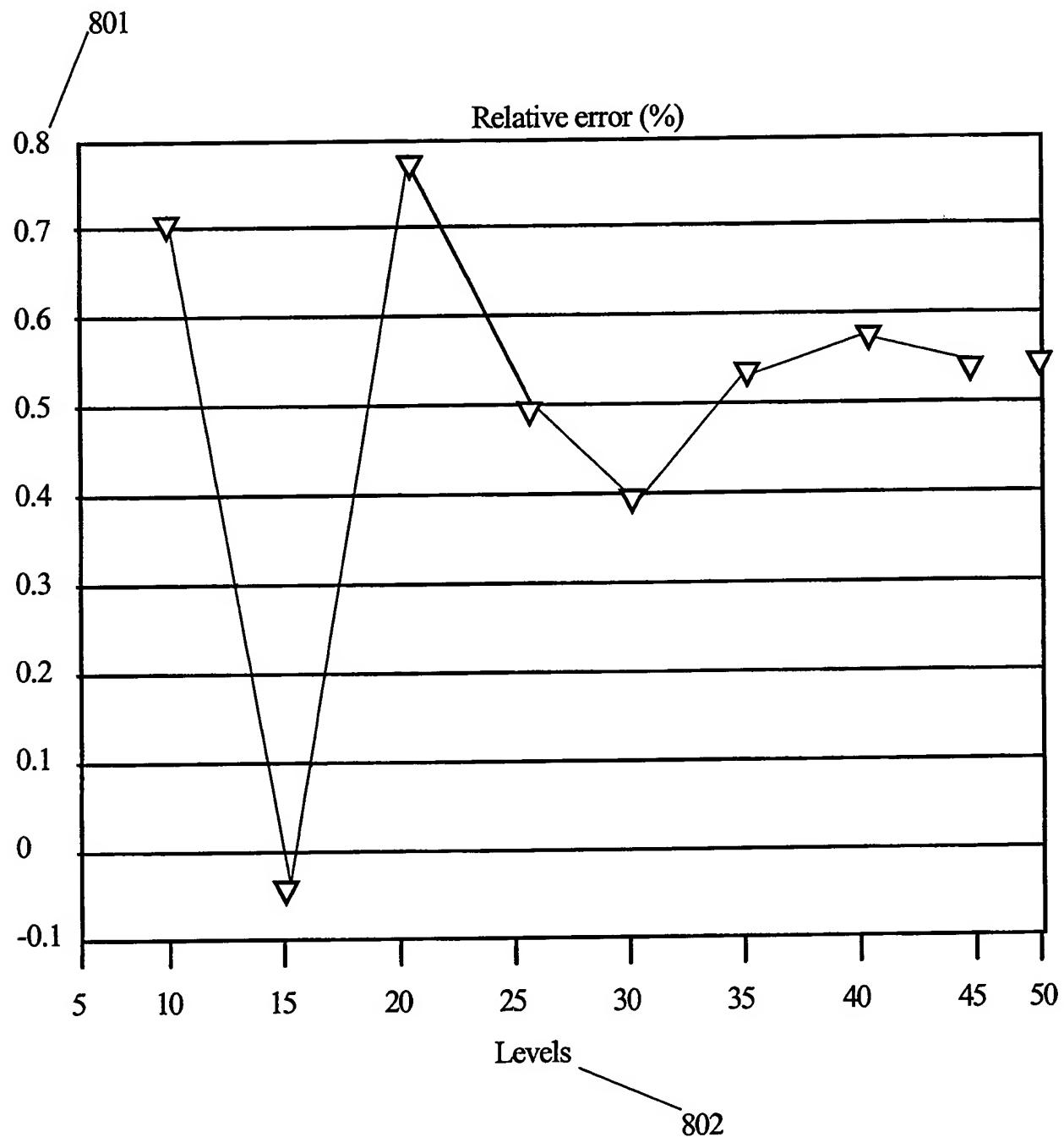


FIG. 8

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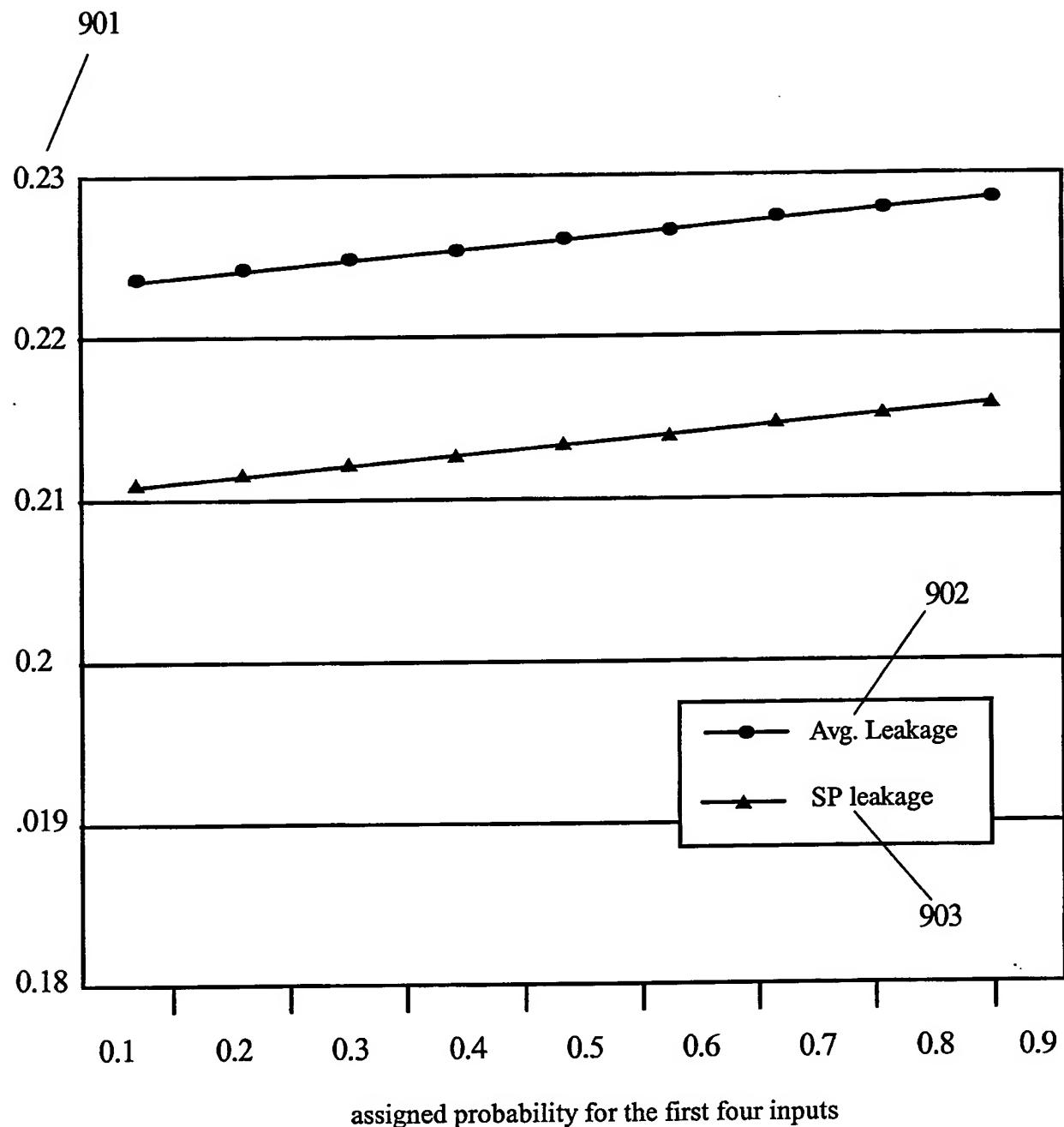


FIG. 9

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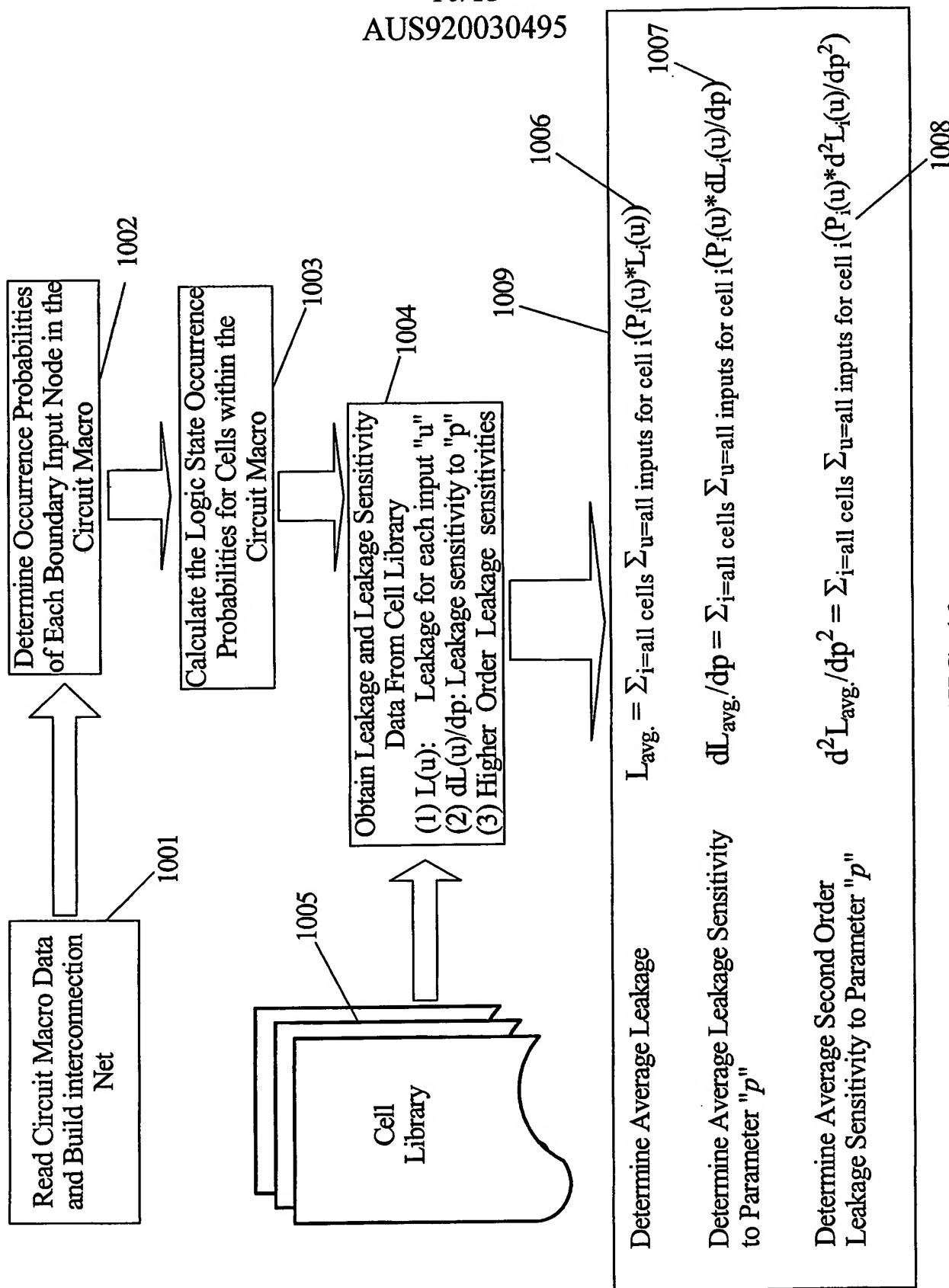


FIG. 10

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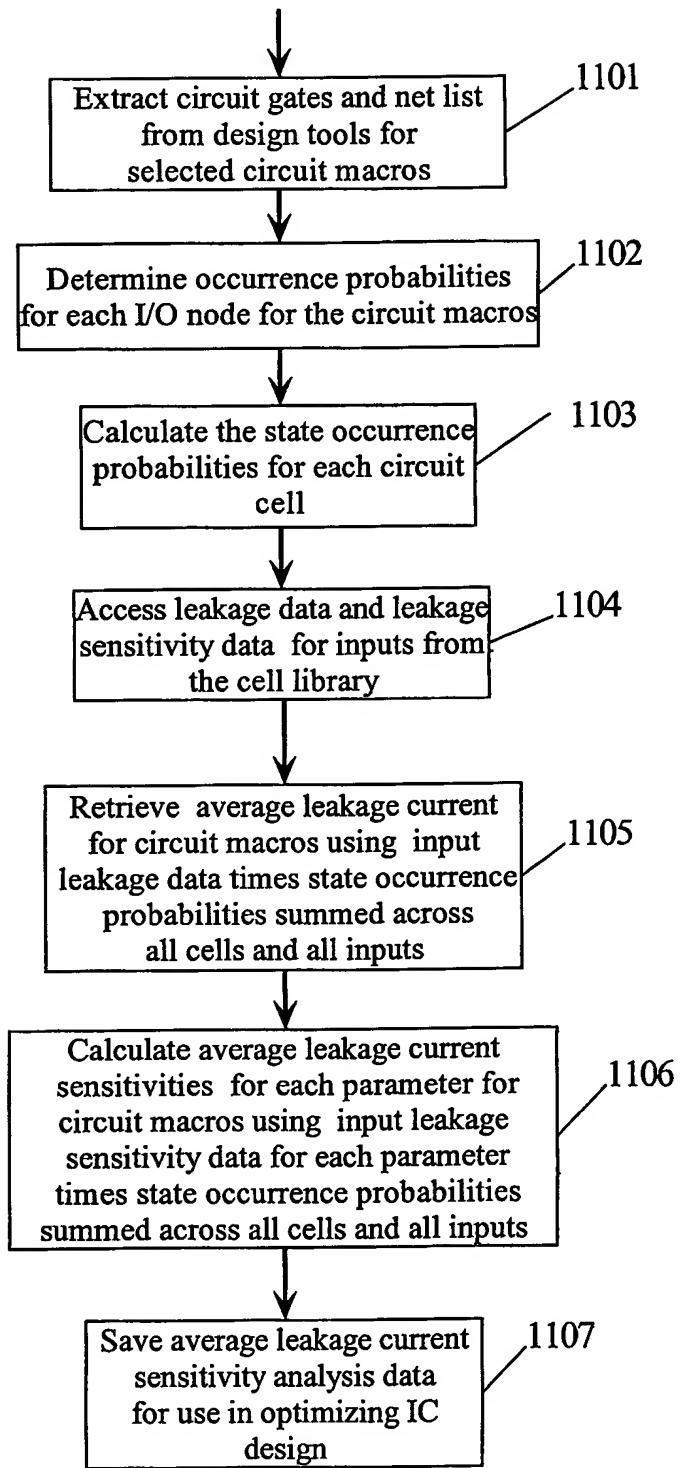


FIG. 11

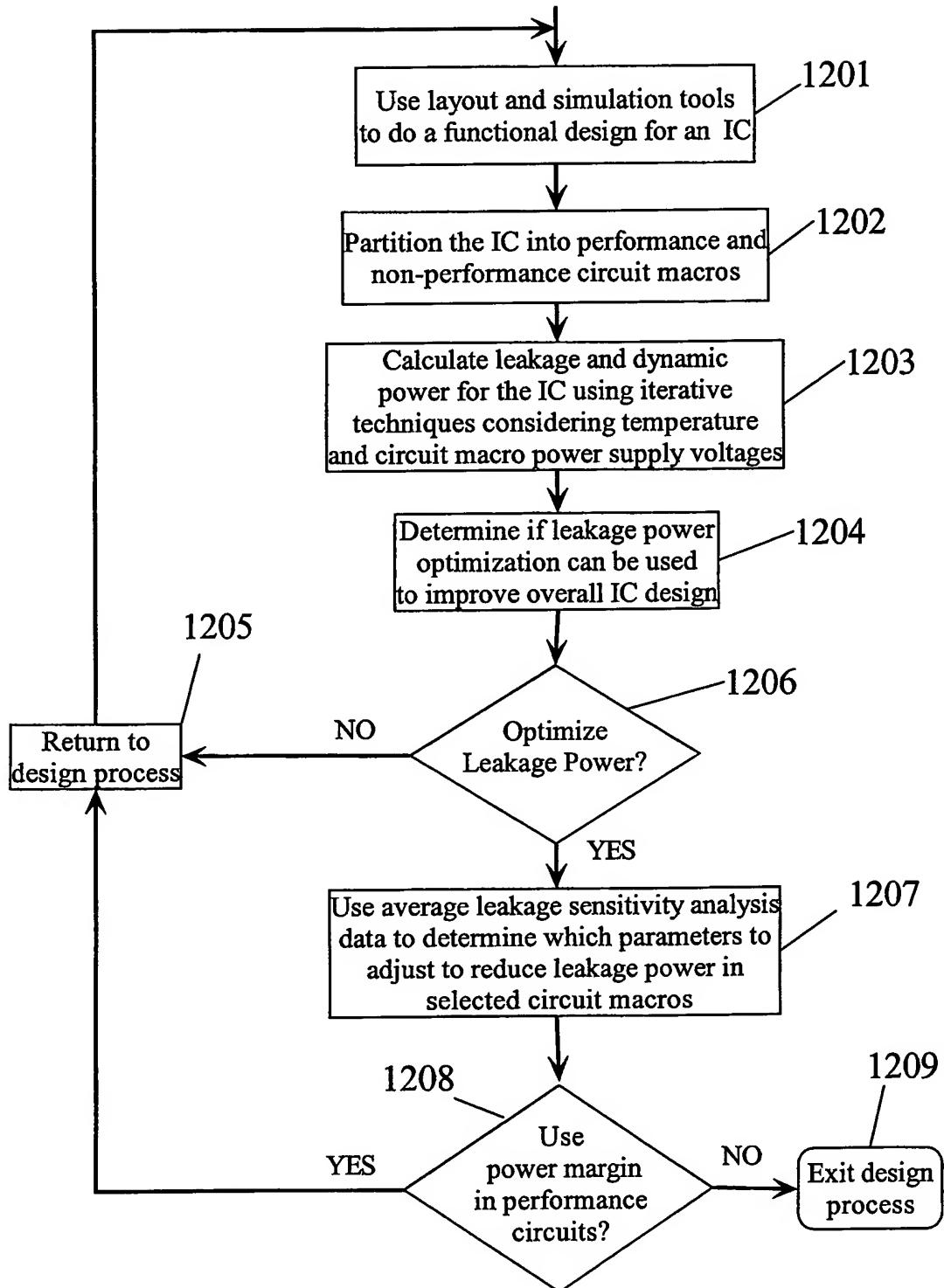


FIG. 12

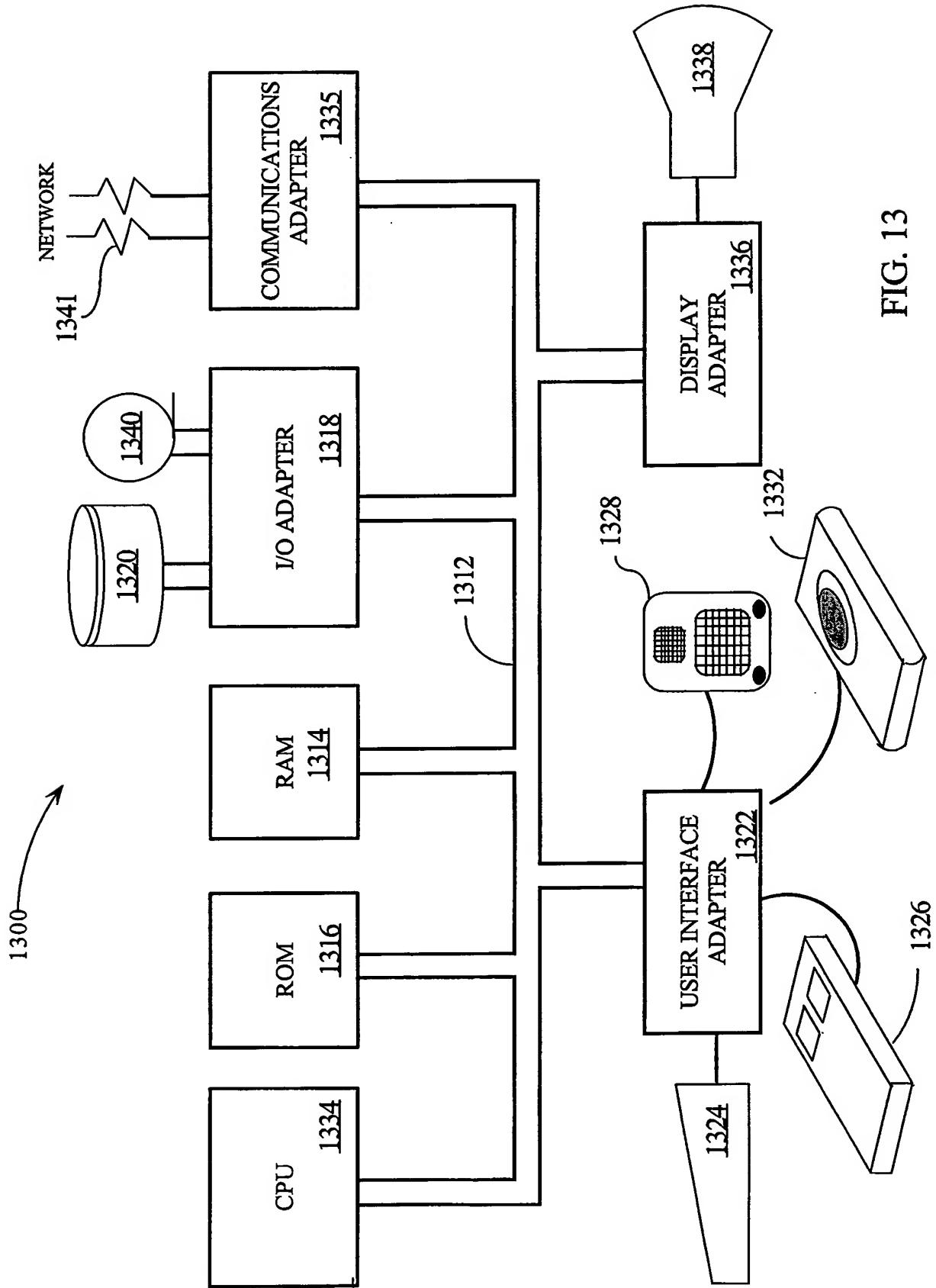


FIG. 13